Fourth Semester Examination, April – 2005

DIGITAL ELECTRONICS CIRCUITS

Full Marks : 70

Time : 3 Hours

The figures in the right hand margin indicate marks for the questions.

Symbols used throughout carry usual meaning. State assumptions clearly in choosing any component value or data if not specified. Group – A is compulsory and answer five questions from Group – B.

Group – A

1. Answer the following : 2×10

(a) Convert $A2F_{16}$ to binary, octal, and decimal.

P.T.O.

(b) Convert 712_8 to binary and binary-coded decimal.

(c) Convert the following decimal numbers to BCD.

(i) 748

(ii) 5668

(d) Explain a simple technique to determine propagation delay of a logic gate.

(e) Construct a truth table for two series inverters; that is, the output of inverter A connects to the input of inverter B. The circuit input is the input of inverter A, while the output of the circuit is the output of inverter B.

(f) How many numbers of NAND gates are required to construct a D Latch ? Sketch the schematic.

(g) Write a VHDL description of a three input NAND gate.

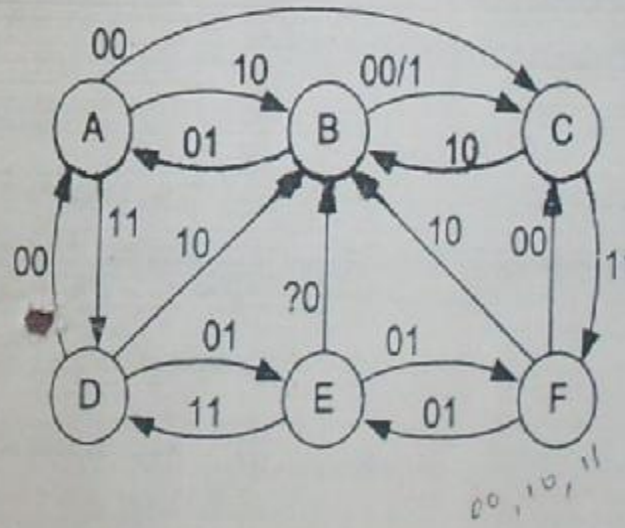
(h) A 4 M-bit memory is partitioned into 32 blocks with each block having 1024 rows and 128 columns. Give the number of bits required for the row address, column address and block address.

(i) Show an example of a function of three variables x, y and z which has more implicants than minterms.

(j) What is the basic difference between SRAMs and DRAMs ?

Group – B

2. Fig. 1 shows the state diagram of a synchronous state machine having two inputs, X and Y and one output, Z. Transitions from a state to itself have been omitted. The symbol "?" denotes "don't care". 2×5



(a) Construct the state table for the state machine including both the next state and the value of the output, Z.

(b) Complete the timing diagram of Fig. 2 by showing the sequence of states that the state machine follows and the waveform of the output signal.

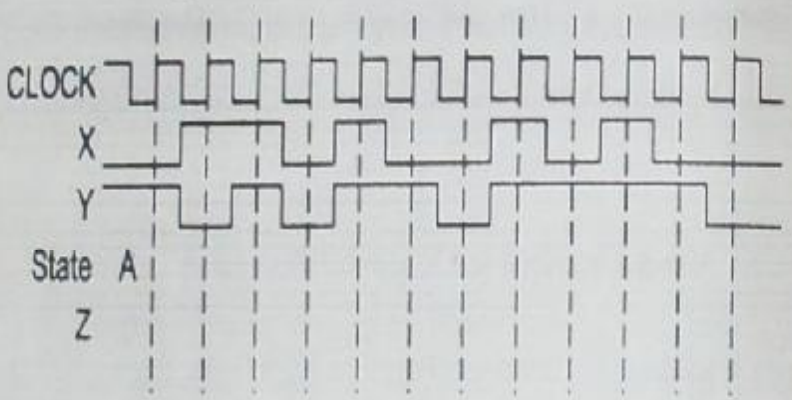


Figure 2

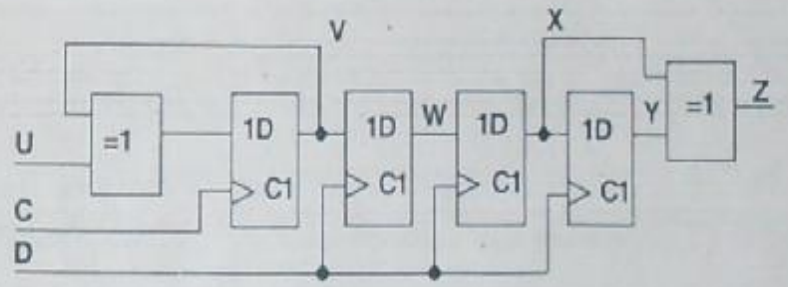
(c) Explain what is meant by saying that two states are "equivalent".

(d) Showing your reasoning clearly, determine which states are equivalent and hence show that it is possible to reduce the number of states to four by merging equivalent states.

(e) Draw a state diagram for the reduced state machine.

3. Fig. 3 shows a circuit containing four flip-flops and two exclusive-or gates. The circuit has two independent clock signals, C and D, which may have different frequencies. The input signal, U, consists of pulses that last exactly one cycle of C and whose transitions occur slightly after the rising edge of C.

$3+2\frac{1}{2}+2\frac{1}{2}+2$



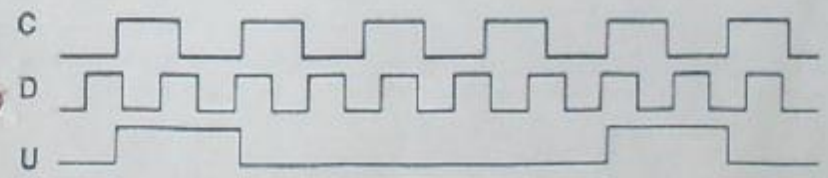


Figure 3

(a) Complete the timing diagram, showing the waveforms of V, W, X, Y and Z. Assume all signals are initially low.

(b) If the clock signals C and D have periods c and d respectively and an arbitrary phase relationshi determine the maximum and minimum time delay between the rising edge of U and the rising edge of the corresponding output pulse at Z. You may neglect propagation delays and setup times.

(c) Determine, as a function of c and d, the minimum interval between successive rising edges of U that will ensure that each input pulse results in a distinct output pulse at Z.

(d) Giving your reasons fully, say which of the signals V, W, X, Y and Z are likely to contain glitches and explain the circumstances under which they may occur.

4. Answer the following : $2\frac{1}{2}\times4$

(a) A positive logic system with logic high defined as any voltage that exceeds 2.4 V and logic low as any voltage under 0.8 V is used. Six successive voltages from most-significant bit to least-significant bit are 2.8 V, 3.4 V, 0.4 V, 3.1 V, 0.6 V, 2.5 V. What binary number is represented by these voltages ? Explain the problem if one of these voltages measured 1.7 V.

(b) Plot the K-map for $Y = AB + A\bar{B} + \bar{A}\bar{B}$.

(c) Reduce to simplest form

$Y = ABC + A\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}D$.

(d) Realize, using NAND gates only, $Y = \bar{A}C + A\bar{B}$.

5. Answer the following : 3+3+4

(a) Plot the K-map for $X = AB + A\bar{B}$.

(b) Realize the expression

$X = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C$ with three 2:1 MUXs.

(d) Design a 4-bit comparator using gates.

6. (a) Write VHDL code for a full subtractor. 5

(b) Write VHDL code for an one bit full adder. 5

7. (a) Design a modulo 16 binary counter with parallel input. 5

(b) Implement a four bit adder using a 512 × 5 ROM module. 5

8. Use flip-flops to design a synchronous counter. Give the VHDL description of the circuit. 10