Total number of printed pages – 8

B. Tech

CPES 5203

Fourth Semester Examination – 2007

DIGITAL ELECTRONICS CIRCUITS

Full Marks – 70

Time : 3 Hours

Answer Question No. 1 which is compulsory and any ***five*** *from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) Carry out the following additions :

   (i) (+ 13, – 11) using 1's complement notation.

   (ii) (– 15, + 9) using 2's complement notation.

(b) (i) Convert $(597)_{10}$ to BCD code.

(ii) Convert 10110111010 to Gray code.

(c) Realize an (i) inverter and (ii) OR gate using NAND gates only.

(d) Use Karnaugh map to reduce $A+B\overline{C}+CD$ to a minimum SOP form.

(e) Develope the logic required to detect the binary code 10010 and produce an active Low output.

(f) (i) Define maximum clock frequency of a Flip-Flop.

(ii) What is set-up time in a flip-flop ?

(g) Distinguish between synchronous and asynchronous counter.

(h) What are the basic memory operations ?

(i) Name the logic family that is most appropriate for each of the following requirements :

(i) Shortest propagation delay time

(ii) Fasted flip-flop toggle rate

(iii) Lowest power dissipation

(iv) Best compromize for speed and power for a logic gate.

(j) What is fan-out ? How do you calculate the fan-out number of a TTL gate ?

2. Using Karnaugh map convert the following standard POS expression into a minimum POS expression, a standard SOP expression and a minimum SOP expression : 10

$$(\overline{A}+\overline{B}+C+D)(A+\overline{B}+C+D)(A+B+C+\overline{D})$$
$$(A+B+\overline{C}+\overline{D})(\overline{A}+B+C+\overline{D})(A+B+\overline{C}+D)$$

Or

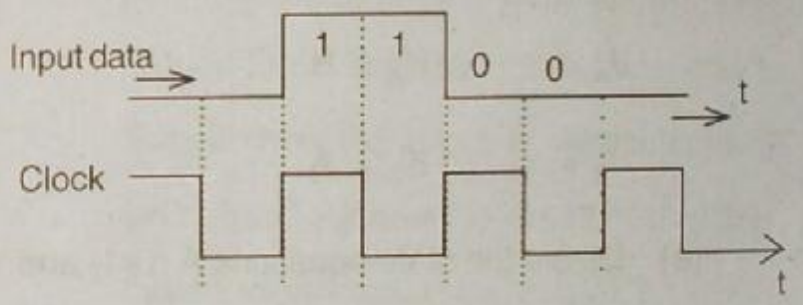
Twelve months of a calender are represented by a 4-bit binary representation, 0001 representing January, 0010 representing February and so on. Design a switching circuit, which will lightup an LED, when fed with input-4-bit pattern, for a month having 30 days. Use minimum number of NAND gates.

3. (a) Write the truth table of a full adder. Draw its complete logic circuit. Add any two two-digit decimal numbers which should result in a carry and explain how the logic circuit functions to register the sum. 5

(b) Obtain the logic diagram for a 1-of-4 multiplexer from its truth table. What will be the logic circuit for the corresponding 1-line to 4-line demultiplexer ? 5

4. (a) With the help of a simplified logic diagram explain the operation of an edge-triggered J.K. flip-flop (FF). Why a pulse transition detector circuit is used in the clock circuit ? How to convert/derive a T-FF form a J-K FF ? 5

(b) Consider a 4-bit serial in/parallel out shift register. Draw its logic diagram. The clock and data waveforms are as given below :



The register initially contains all 1_S. Draw the output waveform. 5

5. (a) Design a MOD-7 counter using J-K FFs. Draw the truth table, the output waveforms and the combination counter circuit you have designed. 5

(b) What is a priority encoder ? Design a priority encoder having D_0 as the highest priority and D_3 as the lowest priority. Write the HDL programme for it. 5

6. A sequential circuit has two J K FFs A and B and one input x. The circuit is described by the following flip-flop input equations :

$J_A = x \qquad K_A = B'$

$J_B = x \qquad K_B = A$

(a) Derive the state equations A (t+1) and B (t+1) by substituting the input equations for the J and K variables. 5

(b) Draw the state diagram of the circuit. 5

7. (a) Draw the logic diagram of a basic ROM programmed for a 4-bit binary-to-Gray conversion. Determine the Gray code output when a binary code of 1011 is applied to the address input lines. 5

(b) Draw in block diagram form the register configuration of a binary multiplier. Two binary numbers 10110 and 10001 are to be multiplied using the above configuration. Draw the corresponding ASM (Algorithmic State Machines) flow chart. Explain how the above multiplication will be carried out and the result of multiplication registered at the output ? 5

8. Answer any *two* of the following : 5×2

(a) Write the HDL programme for functional description of a J K flip-flop

(b) A NAND gate using CMOS logic circuit

(c) Draw the pin diagram of a 64 K × 4 ROM. Use it to form a 64 K × 4 ROM

(d) A 3-bit Magnitude comparator.
