Total number of printed pages – 4

B. Tech

BCSE 3307

Sixth Semester Examination – 2007

COMPUTER ARCHITECTURE AND ORGANIZATION – II

Full Marks – 70

Time – 3 Hours

Answer Question No. 1 which is compulsory and any ***five*** *from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) Why hazards occurs in a pipeline ?

   (b) What do you mean by interrupt latency ?

   (c) Differentiate between multiprocessor and multicomputer.

   (d) Differentiate between loosely coupled and tightly coupled multiprocessor.

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(e) How programmed I/O differs from interrupt driven I/O ?

(f) Define the term 'instruction issue latency'.

(g) What is the need of data forwarding in a pipeline ?

(h) What is the function of DMA ?

(i) What is a super scalar architecture ?

(j) How instruction pipeline differs from arithmetic pipeline ?

2. (a) Describe the Flynn's classification of computer architecture. 5

(b) Explain how a parallel memory allocation attribute to the performance enhancement of SIMD array processor. 5

3. (a) Design a barrel shifter network with 32 number of processing elements. Show the processing elements that are reachable from any one of the processing elements in two steps. 5

(b) Give the comparison of multiprocessor systems with time shared bus, cross-switch and multi port memory. 5

4. (a) Draw the architectural configuration of BSP system. Show how they differs from that of Illiac – IV. 5

(b) A block of data is to be transferred between an I/O device and processor. Explain how this can be accomplished using DMA operation. 5

5. (a) Show the computation of the following Fortran loop in Illiac-IV system for N = 64. 5

```
DO 100 I = 1, N
100 A(I) = B(I) + C(I)
```

(b) Describe the architectural configuration of a SIMD array processor. 5

6. (a) Consider the five-stage pipelined processor specified by the following reservation table : 5

	1	2	3	4	5	6
S1	x					x
S2		x			x	
S3			x			
S4				x		
S5		x				x

(i) List the set of forbidden latencies and the collision vector

(ii) Draw the state transition vector.

(b) A branch instruction causes the pipeline to stall for 3 clock cycle. Give a mecha-

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nism to improve the branch penalty by one clock cycle. 5

7. (a) Find an equation for the Speedup, Efficiency and Throughput of a K-stage linear pipeline. 5

   (b) Explain how data transfer takes place between an I/O device and processor in a program controlled I/O. 5

8. (a) Explain how multiple simultaneous interrupt request is handled by processor. 5

   (b) For the following sequence of code given : 5

   (i) identify the type of hazards

   (ii) instruction involved in the hazard.

LD	R_1, 0(R_2)
DSUB	R_4, R_1, R_5
AND	R_6, R_1, R_7
OR	R_8, R_1, R_9

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