Total number of printed pages – 8 **B. Tech**

CPEC 5403 / BCSE 3407

Seventh Semester Examination – 2007

VLSI DESIGN / VLSI SYSTEM DESIGN

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

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1. (A) Select the correct answer for the following : 1×6

   (i) An *n*-channel MOSFET conducts when it has

   (a) $V_{GS} > V_P$

   (b) An n-type inversion layer

   (c) $V_{DS} > 0$

   (d) Depletion layer.

P.T.O.

(ii) In a CMOS inverter the upper MOSFET is

(a) a passive load

(b) an active load

(c) non-conducting

(d) Complementary.

(iii) The SPICE parameter C_d is the capacitance associated with the

(a) drain of the transistor

(b) depletion region

(c) depth of the channel

(d) none of the above.

(iv) For a CMOS inverter when $V_{in} = V_{th}$

(a) the *n*MOS transistor will be in cut-off while the pMOS transistor will be in saturation.

(b) the *n*MOS transistor will be in linear region while the *p*MOS transistor will be in saturation.

(c) the *n*MOS transistor will be in saturation while the *p*MOS transistor will be in linear region.

(d) both the *n*MOS and *p*MOS transistors will be in saturation.

(v) The propagation delay limit in the CMOS digital integrated circuits is

(a) independent of the doping densities

(b) independent of the channel length

(c) independent of extrinsic capacitance Components C_{int} and C_g .

(d) dependent on the extrinsic capacitance components C_{int} and C_g.

(vi) The high output of a CMOS digital circuit is usually

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(a) $V_{DD}/2$

(b) V_{GS}

(c) V_{Ds}

(d) V_{DD}.

(B) Answer the following questions : 7×2

(a) Draw the circuit diagram and the corresponding stick diagram of a 2-input NAND gate using CMOS technology.

(b) Boundary scan test techniques are grouped by the IEEE standards organisation into a standard access port and boundary scan architecture. Write down atleast four advantages of the Boundary scan test.

(c) Write the specification of an AND gate with constant delay using HDL to simulate the circuit.

(d) Draw the circuit schematic of a (2×1)-multiplexer using CMOS Transmission gates.

(e) With the help of a neat circuit diagram show the implementation of the logic function $Y = A+(B+C).(D+E)$ using domino CMOS logic.

(f) What do you understand by the term Excitation Table ? Show the excitation table of a D Flip-flop.

(g) Using an FPGA discuss the programming required for implementation of a 2-input NOR gate.

2. With the help of suitable diagrams explain the main processing steps involved in the fabrication of an n-channel MOS transistor on a p-type silicon substrate. 10

3. Consider a MOS transistor with the following parameters: $t_{OX} = 200$ Å, $\Phi_{GC} = -0.85$ V, $N_A = 2\times10^{15}\ cm^{-3}$, $Q_{OX} = q.2\times10^{11}\ C/cm^2$.

(a) Determine the threshold voltage V_{T0} under zero-bias atroom temperature(T=300K). Note $\varepsilon_{OX} = 3.97\varepsilon_0$ and $\varepsilon_{si} = 11.7\varepsilon_0$. 6

(b) Determine the type (P-type or n-type) and amount of channel implant (N_i/cm^2) required to change the threshold voltage to 0.8 V. 4

4. (a) Design a circuit described by the function $Y = \frac{}{A.(B+C).(D=E)}$ using CMOS logic. Also find the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left(\frac{W}{L}\right)_p = 5$ for all *p* MOS transistors and $\left(\frac{W}{L}\right)_n = 2$ for all *n* MOS transistors. 5

(b) Derive and calculate the switching threshold voltage V_{th} of the two-input CMOS NOR gate with the following parameters :

$(W/L)_p = 4$, $(W/L)_n = 1$,

$V_{T0n} = 0.7V$, $V_{T0p} = -0.7V$,

$\mu_n C_{ox} = 40\mu A/V^2$, $\mu_p C_{ox} = 20\mu A/V^2$,

$V_{DD} = 5V$, 5

Contd.

5. (a) Derive the current equation using the gradual channel approximation theory for a p-channel MOS transistor operating in the linear region, i.e., for $V_{SG} + V_{Tp} > V_{SD}$. 7

(b) Explain in brief the meanings of regularity, modularity and locality with reference to VLSI design. 3

6. Write the VHDL code for an 8-bit full adder and illustrate the output with suitable diagram. 10

7. (a) Give a brief comparison between Complex Programmable Logic Devices (CPLDs) and Field Programmable Gate Arrays (FPGAs). 6

(b) With the help of a suitable diagram explain a typical CLB available in the FPGAs. 4

8. (a) Discuss how the charge sharing problem can be overcome in dynamic CMOS logic ? 4

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(b) Calculate the values of V_{OH}, V_{OL}, V_{IL} and the noise margin NM_L for a saturated enhancement-load nMOS inverter circuit. Given $V_{DD} = 5.0\,V$, $V_T = V_{T0} = 0.8\,V$ and $k_{driver}/k_{load} = 10$. 6

9. Write short notes on *any two* of the followings : 5×2

(a) Scaling of MOS circuits.

(b) Built-in self-test (BIST)

(c) VLSI design methodology

(d) Layout design rules.

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