 B. Tech

CPEC 5403 / BCSE 3407

Seventh Semester Examination – 2008

VLSI DESIGN / VLSI SYSTEM DESIGN

Full Marks – 70

Time : 3 Hours

Answer Question No. **1** *which is compulsory and any* **five** *from the rest.*

The figures in the right-hand margin indicate marks.

1. (i) Select the correct answers for the following questions from the choice given : 1 × 6

(a) For a small value of V_{DS} the channel in MOSFET is ;

(i) not formed

(ii) a linear resistor whose value is controlled by V_{GS}.

(iii) pinched off

(iv) enhanced.

(b) One of the immediate challenges in miniaturisation of IC's in microelectronics fabrication technology is in

(i) metallization

(ii) gate.

(iii) source.

(iv) drain.

(c) When positive charge on its gate turns the channel of an n-channel MOSFET into n-type semiconductor, all three parts of the MOSFET (source, channel, and drain) are n-type. As a result,

(i) the MOSFET becomes highly magnetic, with its north pole on its source and its south pole on its drain.

(ii) the MOSFET becomes highly magnetic, with its south pole on its source and its north pole on its drain.

(iii) current flows easily through the MOSFET, from source to drain.

(iv) no current can flow through the MOSFET.

(d) If we set the inputs of a particular CMOS gate to voltages that correspond to valid logic levels, we would expect the *static* power dissipation of the gate to be

(i) zero

(ii) non-zero but very small (picowatts).

(iii) Depends on whether output voltage is low or high.

(iv) Unknown with the facts given.

(e) To *decrease* the output rise time of a CMOS gate one could

(i) increase the length of all *p*-MOSFETs.

(ii) increase the length of all *n*-MOSFETs.

(iii) increase the width of all *p*-MOSFETs.

(iv) increase the width of all *n*-MOSFETs.

(v) none of the above.

(f) A variable is assigned a value using the variable assignment statement in VHDL, which has the general form as :

(i) Variable-object : expression

(ii) Variable-object : = expression

(iii) Variable-object = expression

(iv) none of the above.

(ii) Give the transistor schematic and stick diagram for a static CMOS 2-input NOR gate. 2

(iii) Consider the logic expression out = $\overline{a \cdot b + c \cdot d}$. Convert this to a suitable electrically equivalent transistor-level schematic diagram using CMOS logic. 2

(iv) Draw and label the energy band diagrams of metal, oxide and semiconductor layers in a MOS system as three separate components. 2

(v) Write the symbol, SPICE keyword and typical values of the Zero bias bulk

capacitance per square meter and Drain ohmic resistance of a typical MOS Transistor. 2

(vi) How many devices can be fabricated on a 4 inch Silicon wafer by using 2 μm technology ? 2

(vii) Implement a two input MUX circuit using Transmission Gate. 2

(viii) The threshold voltage of an enhancement-type n-channel MOSFET is a positive quantity, whereas the threshold voltage of a p-channel MOSFET is negative, why ? 2

2. (a) Draw a transistor-level circuit diagram of a 2-input NAND gate in CMOS and describe its operation in brief. 5

(b) Sketch a stick diagram and physical layout for the same gate, paying attention to the dimensions of the transistors to ensure balanced rise and fall times. 5

3. Consider the design of a 16-input AND gate in static CMOS.

(a) Explain why the 2-input design could not simply be scaled up. 3

(b) Sketch alternative designs using two and four levels of NAND and NOR gates. 7

4. (a) Write the VHDL code for an 8-bit full adder and illustrate the output with suitable diagram. 6

(b) Write the VHDL code of a counter which counts from 1 to 15. 4

5. (a) Discuss the operation of CMOS inverter by drawing its VTC and derive the expression for its switching threshold voltage and show that for a symmetric inverter $(W / L)_p = 2.5\ (W / L)_n$. 5

(b) Implementation of the Boolean expression, $Z = (A + B + C) \cdot (D + E)$ using CMOS and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that $(W/L)_p = 15$ for all pMOS transistors and $(W/L)_n = 10$ for all nMOS transistors. 5

6. (a) Design a 2 ×1 multiplexer using CMOS transmission gate. 2

(b) Implement the function Y=A+(B+C) • (D+E) using domino CMOS logic. 3

(c) With the help of a suitable diagram explain a typical CLB available in the FPGAs. 5

7. (a) Draw the energy band diagrams of MOS system under external Bias. 3

(b) Consider the following *n*-channel MOSFET process: Substrate doping

$N_A = 10^{16}\ cm^{-3}$, poly silicon gate doping density $N_D = 2 \times 10^{20}\ cm^{-3}$, gate oxide thickness $t_{ox} = 500A°$ and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}\ cm^{-2}$. Calculate the threshold voltage (V_{TO}) and determine the type and the amount of channel ion implant which are necessary to achieve a threshold voltage of 1V. 7

(Assume $\Phi_F(gate) = 0.55\,V, \varepsilon_{si} = 11.7\varepsilon_O$, $\varepsilon_{ox} = 3.97\varepsilon_O$, $n_i = 1.45 \times 10^{10}\ cm^{-3}$).

8. Answer any *two* of the followings : 5×2

(a) Explain briefly the VLSI design flow by plotting Gajski's Y chart.

(b) With the help of a simplified process sequence flow diagram explain the fabrication of the n-well CMOS integrated circuit with single poly-silicon layer.

(c) State and explain briefly some of the important design styles used for VLSI chip design and implementation.

(d) What is need of scaling ? Explain the limitations of constant voltage scaling.

(e) Write a short note on BIST.