Total number of printed pages – 8 **B. Tech**

CPES 5203

Fourth Semester Examination – 2008

DIGITAL ELECTRONICS CIRCUITS

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*

The figures in the right-hand margin indicate marks.

1. Answer the following questions : 2×10

   (a) What are the maximum positive and negative numbers that can be represented by 4-bit binary number using

      (i) 1's complement notation and

      (ii) 2's complement notation

   (b) _____ is a self complementing code and _____ is an un-weighted code.

   (c) Find the complement of $F = x + yz$; then find the values of $F \bullet F'$ and $F + F'$.

   (d) What do you mean by "Prime Implicants" in a Karnaugh map ? Under what condition a min-term in a square is said to be essential ?

   (e) Draw the circuit diagram and truth table of

      (i) 3 -bit even parity generator and

      (ii) 4-bit even parity checker.

   (f) Distinguish between Decoder, Encoder and Multiplexer in digital circuits.

   (g) What do you mean by 3-state gate ? What is it's importance in combinational circuit ?

   (h) What do you mean by Sequential Logic Circuit ? Hence distinguish between

Synchronous Sequential Logic Circuit and Asynchronous Sequential Logic Circuit.

(i) How many 32K × 8 RAM chips are needed to provide a memory capacity of 256 K bytes ? How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips ?

(j) How "FAN OUT" of a gate is specified ?

2. (a) Explain in brief different types of graphic and control characters in ASCII Character Code. 3

(b) What is the decimal equivalent of the binary number (1000 1011 0111) represented in Excess-3 code ? 1

(c) What bit must be complemented in the ASCII Character Code to change letters from capital to lower case ? 1

(d) Simplify the following expression using Boolean algebra. 2

$A'B(A'+C'D)+B(A+A'CD)$

(e) Obtain the truth table of the following function and express in Sum-of-minterms and Product-of-maxterms. 3

(xy + z) (y + xz)

3. (a) Simplify the following Boolean function using five-variable map. $2\frac{1}{2}$

$F = A'B'CE' + A'B'C'D' + B'D'E' + B'CD' + CDE' + BDE'$

(b) Draw a NAND logic diagram that implements the following function. $2\frac{1}{2}$

$F = (AB + A'B')(CD' + C'D)$

(c) Implement the following Boolean function using NAND-AND two level combinational form $2\frac{1}{2}$

$F(A, B, C, D) = \sum 0, 1, 2, 3, 4, 8, 9, 12$

(d) Implement the following Boolean expression with XOR and AND gates. $2\frac{1}{2}$

$$F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$$

4. (a) Describe the principle of ''Carry Look-ahead'' technique. Write the Boolean function and draw the logic diagram of a 4-bit Carry Look-ahead generator. Now construct a 4-bit adder with Carry Look-ahead. 5

b) A magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether $A > B$, $A = B$ or $A < B$. Determine the algorithm to implement this comparator and draw a 4-bit magnitude comparator using combinational circuit. 5

5. (a) Describe the construction and operation of a Master-Slave flip-flop. 2

(b) Explain how an Edge-triggered D flip-flop can be constructed using SR Latches. 3

(c) A sequential circuit has two JK flip-flops *A* and *B,* two inputs *x* and *y,* and one output z. The flip-flop input equations and circuit output equations are,

$$J_A = Bx + B'Y' \qquad K_A = B'xY'$$

$$J_B = A'x \qquad K_B = A + xy'$$

$$z = Ax'y' + Bx'y'$$

Draw the logic diagram of the circuit. Write the state table and derive the state equations for *A* and *B.* 5

6. (a) Write the state diagram of 4-bit BCD ripple counter. Draw a 4-bit asynchronous BCD ripple counter using any suit-

able flip-flop and explain how the output changes with each clock pulses. Explain how a synchronous BCD ripple counter can be constructed using T flip-flop and draw the circuit diagram. 5

(b) Design a counter with the following repeated binary sequence : 0, 1, 2, 4, 6. Use D flip-flops. 5

7. (a) Explain how a single 2 × 4 decoder can be used to construct a 4 × 4 RAM. $2\frac{1}{2}$

(b) How coincident decoding is used to construct a 1K-word memory using two 5 × 32 **decoder** ? $2\frac{1}{2}$

(c) Describe the techniques used in Address Multiplexing in DRAM. $2\frac{1}{2}$

(d) Describe basic configurations of Programmable Logic Devices. Which one is the most flexible PLD ? $2\frac{1}{2}$

8. Write a brief note on any *two* : 5+5

(a) Sequential Programmable Device

(b) Basic structure of MOS transistor, Symbols of p-channel and n-channel transistors and implementation of an Inverter circuit.

(c) Emmiter Coupled Logic

(d) Hardware Description Language.

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